

12. (Amended) An electrically conductive layer comprising:

a copper alloy which includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight,

wherein the mass-transfer of copper is suppressed through said copper alloy,

wherein said copper alloy further includes at least one of Ag, As P, Si, Bi, Sb, and Ti in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper, and

wherein said copper alloy further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit of copper.

22. (Amended) A semiconductor device comprising:

a semiconductor substrate;

an insulation layer over said semiconductor substrate, and said insulation layer having a trench groove;

a barrier metal layer on a bottom and side walls of said trench groove; and

an electrically conductive layer provided in an interconnection layer on said barrier metal layer, and said interconnection layer filling said trench groove,

wherein said interconnection layer comprises a copper alloy which includes at least one of Ag, As P, Si, Bi, Sb, and Ti in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper, so that said copper alloy is in a solid solution,

wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight, and

wherein said copper alloy further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

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57. (Amended) An electrically conductive layer comprising:

a copper alloy which includes at least one of Ag, As P, Si, Bi, Sb, and Ti at more than 0.2 percent by weight,

said copper alloy formed on a substrate of a semiconductor circuit,

wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight, and

wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

58. (Amended) An electrically conductive layer comprising:

a copper alloy which includes at least one of Ag, As P, Si, Bi, Sb and Ti at not less than 0.1 percent by weight,

said copper alloy formed on a substrate of a semiconductor circuit,

wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight, and

wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

59. (Amended) An electrically conductive layer comprising:

a copper alloy which includes at least one of Ag, As P, Si, Bi, Sb, and Ti in a range of

not less than 0.1 percent by weight to not more than a maximum solubility limit to copper, so that said copper alloy is in a solid solution,

said copper alloy formed on a substrate of said semiconductor circuit,

wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight, and

wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

60. (Amended) An electrically conductive layer comprising:

a copper alloy which includes at least one of Ag, As P, Si, Bi, Sb, and Ti at not less than 0.1 percent by weight and at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight,

wherein said copper alloy has a melting point less than copper and the mass-transfer of copper is suppressed through said copper alloy,

wherein said copper alloy further includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight, and

wherein said copper alloy further includes at least one of Cr and Ni in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

61. (Amended) An electrically conductive layer provided in a semiconductor circuit comprising:

a copper alloy which includes at least one of Ag, As P, Si, Bi, Sb, and Ti at not less than 0.1 percent by weight,

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CS  
said copper alloy provided in a groove within an inter-layer formed on a substrate of  
said semiconductor circuit,

wherein said copper alloy further includes at least one of Mo, Ta and W in a range  
of not less than 0.1 percent by weight to not more than 1 percent by weight, and

wherein said copper alloy further includes at least one of Cr and Ni in a range of  
not less than 0.1 percent by weight to not more than 1 percent by weight.

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**Please add the following new claim:**

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- - 64. (New) The semiconductor device according to claim 1, wherein said copper alloy  
further includes at least one of Ge and Mg in a range of not less than 0.1 percent by weight to  
not more than 1 percent by weight.- -

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**REMARKS**

Claims 1, 2, 4, 6-12, 15-25, 28-37, and 57-64 are all claims presently pending in the  
application. New claim 64 has been added to more particularly define the invention. Claims  
3, 5, 13, 14, 26, and 27 have been canceled without prejudice or disclaimer. Claims 1, 12,  
22, and 57-61 have been amended. Claims 1-37 and 57-63 stand rejected under 35 U.S.C. §  
103(a) as being unpatentable over Edelstein (U.S. Pat. No. 6,181,012 B1) or Dubin (U.S. Pat.  
No. 6,249,055 B1) taken with any Kato (Jap. No. 63-262437), Oyama (Jap. No. 3-285,035),  
Yamasaki, et al. (U.S. Pat. No. 4,559,200) and further in view of Tsuji et al. (U.S. Pat. No.  
5,004,520). Reconsideration is respectfully requested. These rejections are respectfully  
traversed in view of the following discussion.

Attached hereto is a marked-up version of the changes made to the specification